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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,237	12/12/2003	Han-Wook Hwang	8733.713.10-US	9469

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EXAMINER	
ZARABIAN, AMIR	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/733,237	HWANG, HAN-WOOK
	Examiner	Art Unit
	Olivia T. Luk	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 3/15/04 was filed after the mailing date of the application on 12/12/03. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 10-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Miyake et al. (6,788,108 B2).

In re claim 10, Miyake et al. discloses forming a poly-crystalline semiconductor layer **5003 to 5005** on a buffer layer **5002** on a substrate **5001** (col. 12, lines 38-55); forming a gate insulation layer **5006** over the poly-crystalline semiconductor **5003 to 5005** (col. 13, lines 30-35), wherein the gate insulation layer is formed with a first thickness at a channel position and at source and drain positions (see figures 7a-c and 8a-c), wherein the gate insulation layer is formed with a second thickness at offset positions, and wherein the thickness of the gate insulation layer tapers in sequential doping positions from the second thickness to the first thickness; forming a gate structure (see figures 7-8) on the gate insulation layer, wherein the gate structure includes a main gate electrode over the channel position and auxiliary gate electrodes over the offset

positions; impurity doping the semiconductor layer through exposed portions of the gate insulation layer while using the gate structure as a mask to define sequential doping regions that are aligned with the sequential doping positions (col. 14, lines 40-54), and source and drain regions that are aligned with the source and drain positions.

In re claim 11, Miyake et al. discloses further including forming an interlayer **5032** over the gate insulation layer and over the gate electrode; and forming contact holes through the interlayer to expose the source and drain electrodes (col. 16, lines 38-43).

In re claim 12, Miyake et al. discloses forming drain and source electrodes that contact the source and drain regions through the contact holes (col. 16, lines 38-43 and figures 8a-c).

In re claim 13, Miyake et al. discloses forming a poly-crystalline semiconductor layer **5003 to 5005** includes depositing a poly-crystalline silicon on the buffer layer **5002** (col. 12, lines 51-60).

In re claim 14, Miyake et al. discloses forming a poly-crystalline semiconductor layer **5003 to 5005** includes depositing the buffer layer **5002** on a glass substrate **5001** (col. 12, lines 38-60).

In re claim 15, Miyake et al. discloses depositing an amorphous silicon (col. 12, line 51) on the buffer layer **5002**, and laser-annealing the amorphous silicon (col. 12, lines 51-55).

In re claim 16, Miyake et al. discloses forming a first insulation layer **5006** on the poly-crystalline semiconductor layer **5503 to 5005**; forming a second insulation layer on the first insulation layer **5031**, and etching the second insulation layer (col. 16, lines 28-43).

In re claim 17, Miyake et al. discloses impurity doping the semiconductor layer includes forming an impurity concentration in the sequential doping region that depends on the taper of

the gate insulation layer in the sequential doping positions (bridging paragraph of col. 15 and col. 16; see figures 8a-c).

In re claim 18, Miyake et al. discloses forming a passivation layer **5032** over the source and drain electrodes and over the interlayer .

In re claim 19, Miyake et al. discloses forming a drain contact hole through the passivation layer, wherein the drain contact hole exposes the drain electrode (col. 16, lines 38-44).

In re claim 20, Miyake et al. discloses forming a drain contact electrode on the passivation layer, wherein the drain contact electrode contacts the drain electrode through the drain contact hole (col. 16, lines 38-44).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References not applied are considered state of the art in the area of semiconductor manufacture.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Olivia T. Luk whose telephone number is 571-272-1676. The examiner can normally be reached on 8AM to 5PM Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER

OTL
March 22, 2005